REMARKS

Applicant affirms Applicant's election of Claims 1-10.

The Examiner rejected Claims 1, 3, 5 and 7 under 35 U.S.C. 102(b) as being anticipated by Cambou, *et al* (hereafter "Cambou")(US 5,091,330). Applicant traverses this rejection. The Examiner has the burden of showing by reference to the cited art each claim limitation in the reference. Anticipation under 35 U.S.C. 102 requires that each element of the claim in issue be found either expressly or inherently in a single prior art reference. *In re King*, 231 USPQ 136, 138 (Fed. Cir. 1986); *Kalman v. Kimberly-Clark Corp.*, 218 USPQ 781, 789 (Fed. Cir. 1983). The mere fact that a certain thing may result from a given set of circumstances is not sufficient to sustain a rejection for anticipation. *Ex parte Skinner*, 2 USPQ2d 1788, 1789 (BdPatApp&Int 1986). "When the PTO asserts that there is an explicit or implicit teaching or suggestion in the prior art, it must indicate where such a teaching or suggestion appears in the reference" (*In re* Rijckaert, 28 USPQ2d, 1955, 1957). Under the doctrine of inherency, if an element is not expressly disclosed in a prior art reference, the reference will still be deemed to anticipate a subsequent claim if the missing element "is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *Cont'l Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749(Fed. Cir. 1991). "Inherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." Trintec Indus., Inc. v. Top-U.S.A. Corp., 295 F.3d 1292, 1295, 63 USPQ2d 1597, 1599(Fed. Cir. 2002) (quoting *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)).

In making this rejection, the Examiner identifies the trenches shown at 13 and 14 in Figures 1-5 of Cambou as the vias. Applicant respectfully disagrees, a trench is not a via. A "via" in the integrated circuit arts is a hole used as a pass through. The trenches identified by Cambou are isolation trenches for isolating circuitry that is fabricated on the island 18 from circuitry fabricated on island 19 shown in Figure 5.

In addition, Applicant must point out that even if one were to make the correspondence between the trenches of Cambou and the vias of Claim 1, the trenches are on the wrong side of the substrate. Claim 1 requires that the trenches extend from the surface of the substrate on which the integrated circuit components are constructed. Cambou teaches that the integrated circuit components, e.g. elements 31 and 32 in Figure 8, are formed on the surface opposite to that in which the trenches are cut. Hence, Cambou fails to teach two of the limitations of Claim 1 or the claims dependent therefrom.

With reference to Claim 5, the Examiner has not pointed to any teaching in Cambou that the vias are filled with an electrically conducting material. In fact, Cambou teaches that the trenches identified by the Examiner are filled with a planarizable dielectric material, not an electrically conducting material. Accordingly, there are additional grounds for allowing Claim 5.

With reference to Claim 7, Applicant repeats the arguments made above with reference to the claimed anticipation of Claim 1. In addition, the Examiner has not pointed to any teaching in Cambou of a dielectric layer having top and bottom surfaces, said dielectric layer covering said circuit layer such that said bottom surface is in contact with said integrated circuit layer and a plurality of electrical conductors buried in said dielectric layer and making electrical connections to said integrated circuit elements. Hence, there are additional grounds for allowing Claim 7.

The Examiner rejected Claims 1-2 and 7-10 under 35 U.S.C. 102(e) as being anticipated by Nakano, *et al* (hereafter "Nakano")(US 2001/0030366). Applicant traverses this rejection.

In making this rejection, the Examiner looks to Figures 10a-10h of Nakano. Specifically, the Examiner identifies layer 10a as the wafer material having a circuit layer constructed thereon. The Examiner points to paragraph 4 as disclosing the circuit layer. The Examiner identifies layer 3 as the bottom layer of the via and states that this layer is "inherently" more resistant to CMP than the wafer material.

First, paragraph 4 of Nakano does not describe the elements of Figures 10a-10h. Referring to paragraph 6 of Nakano, Figure 10a shows the upper wiring layer of an integrated circuit. That is, the integrated circuit elements are constructed on a substrate that is below this layer and not shown.

Furthermore, even if one were to assume that the conductors shown in Figure 10a were the integrated circuit elements, the via having layer 3 as the bottom surface thereof does not extend from the first surface into the substrate. The via in question extends from the top surface of the dielectric layer 4 to the top surface of the substrate.

Third, there is no teaching with respect to the relative resistance of the alloy used for layer 3 and the substrate identified by the Examiner. Inherency requires that the relative resistance always be the as claimed. The Examiner has the burden of showing that the relative resistance is always as claimed. Hence, Applicant submits that the Examiner has not made a *prima facia* case for anticipation with respect to Claims 1 and 7 or the claims dependent therefrom.

With reference to Claim 3, the Examiner has not pointed to any teaching in Nakano that the vias are lined with an electrically insulating material. Since the via identified by the Examiner must make an electrical connection to the underlying wiring layer shown at 2b, the vias taught in Nakano could not have this property, since such a layer would prevent the electrical connection in question. Hence, there are additional grounds for allowing Claim 3.

The Examiner rejected Claims 1, 3 and 4 under 35 U.S.C. 102(e) as being anticipated by Kim, *et al* (hereafter "Kim")(US 6,461,937).

In making this rejection, the Examiner identifies the trench shown in Figure 17 as the "via" which is lined with an electrically insulating material, i.e., silicon dioxide. The Examiner identifies layer 212, which is a silicon nitride stress relief layer as the layer having the required resistance to CMP.

As noted above, Applicant maintains that the trench is not a via. Furthermore, the Examiner has not pointed to any teaching in Kim that the silicon nitride layer 212 is more resistant to CMP than the underlying substrate. Hence, Applicant submits that the Examiner has not made a *prima facia* case for anticipation with reference to Claim 1 and the claims dependent therefrom.

The Examiner rejected claims 1, 3, 5 and 6 under 35 U.S.C. 102(e) as being anticipated by Lopatin, *et al* (hereafter "Lopatin") (US 6,433,379).

In making this rejection, the Examiner looks to Figures 1-3 of Lopatin and identifies the trenches shown at 30 as the vias. As noted above, a trench is not a via. Accordingly, Applicant submits that the present invention is not anticipated by Lopatin.

I hereby certify that this paper is being sent by FAX to 703-872-9318.

Respectfully Submitted,

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